UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,793	07/02/2003	Arup Bhattacharyya	1303.111US1	5437

21186 7590 08/07/2009

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
08/07/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@slwip.com
request@slwip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/612,793
Filing Date: July 02, 2003
Appellant(s): BHATTACHARYYA, ARUP

Thomas L. Dickey
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 05/12/2009 appealing from the Office action mailed 02/03/2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is deficient. 37 CFR 41.37(c)(1)(v) requires the summary of claimed subject matter to include a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by page and line number, and to the drawing, if any, by reference characters. The brief is deficient because:

In his summary Appellant characterizes every independent claim on appeal as including an n/i/p diode that is required to have no gate; however, the summary refers to Figures (1B, 2B, 3B, 4B, and 5B) showing n/i/p diodes that have gates.

1. In his brief, Appellant characterizes each of independent claims 1, 6, 7, 20, 33, 63, and 72 with the exact same words, "The diode includes an anode 104, 204, 304, 404, 504, a cathode 103,203, 303,403,503 and an

intrinsic region (i) between the anode and the cathode [, and] has a structure to allow the memory cell to switch memory states … without gating the diode (see for example, page 9 lines 2-4 and lines 22-23)". See page 6 lines 20-21, page 7 lines 10-11 and 27-28, page 8 lines 14-15, page 9 lines 4-5 and 20-21, and page 10 lines 13-14 of the Appeal Brief.

2. Note that the passage cited in the brief (page 9 line 22-23 of the specification) reads, "However, the performance of CED-RAM cells without gate-controlled diodes is sufficient for many applications."
3. On 7/9/08, claims 1, 6, 7, 20, 33, 63, and 72 were each amended using the same language: "wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode".
4. This claim language was added in response to a rejection that found the un-amended claims obvious in view of Baba 5,686,739, which discloses an n/i/p negative resistance diode (with an intrinsic region 4 between an anode 8 and a cathode 9) that has a structure that allows the diode to switch states using a forward or reverse bias voltage, as shown in figure 2, and a negative resistance response, as shown in figure 3 of Baba.
5. Baba's NDR diode also has gate 7, a fact Appellant pointed on page 22 of his response filed 7/9/08. On that date, Appellant wrote, "In contrast [to Baba], Applicant claims a diode [where] a diode gate is not necessary to switch states."

In view of Appellant's present characterization ("The diode … has a structure to allow the memory cell to switch memory states … without gating the diode") of the claims, as well as Appellant's 7/9/08 characterization ("In contrast [to Baba], Applicant claims a diode [where] a diode gate is not necessary to switch states.") of the claims, it appears to have been Appellant's intent for the claim language, "without gating the diode" to avoid Baba by limiting the claimed invention to the un-gated (see page 10 line 2 and page 11 lines 26-28 of the specification) embodiments of figures 1A, 2A, 3A, 4A, and 5A.

In light of this fact, Figures 1B, 2B, 3B, 4B, and 5B, which show diodes that (in Appellant's 7/9/08 words) contrast to the claims on appeal by having gates, do not belong in a summary of the claimed invention.

Certain of Appellant's arguments seem to rely on characterizing the claimed invention as including Figures 1B, 2B, 3B, 4B, and 5B's gated NDR n/i/p diode (to avoid the un-gated n/i/p NDR diode of Krivokapic 6,291,832) while still requiring the claimed invention to include Figures 1A, 2A, 3A, 4A, and 5A's ungated NDR n/i/p diode (thus still avoiding Baba's (previously-cited) gated NDR n/i/p diode). If it were possible for the claimed invention to avoid Baba by including an un-gated NDR n/i/p diode while simultaneously avoiding Krivokapic by including a gated NDR n/i/p diode, this appeal would be unnecessary. However, Appellant seems to have specifically limited his claimed invention to the ungated embodiments of Figures 1A, 2A, 3A, 4A, and 5A.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,229,161	Nemati et al.	05-2001
6,291,832	Krivokapic	09-2001
5,686,739	Baba	11-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

Claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over NEMATI ET AL. (6,229,161) in view of KRIVOKAPIC (6,291,832). In the examiner's opinion, this/these claim(s) would have been obvious according to one of the rationales expressed in the *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International Co. v. Teleflex Inc.*, as published at 72 Federal Register 57526 et seq.[1] (10/10/2007).

The Guidelines explain that an invention that would have been obvious to a person of ordinary skill at the time of the invention is not patentable. The Guidelines point out that, as reiterated by the Supreme Court in KSR, the framework for the

[1] Available at http://www.uspto.gov/web/offices/com/sol/notices/72fr57526.pdf See also MPEP, Eighth Ed. Rev. 6 (Sept. 2007) §§ 2141 et seq., available at http://www.uspto.gov/web/offices/pac/mpep/documents/2100.htm Please note that §§ 2141 et seq. have been completely revised, in view of KSR v. Teleflex.

objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.* Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court are as follows:

(1) Determining the scope and content of the prior art;

(2) Ascertaining the differences between the claimed invention and the prior art, and

(3) Resolving the level of ordinary skill in the pertinent art.

Examining this last factor first, it is noted that any obviousness rejection should include, either explicitly or implicitly in view of the prior art applied, an indication of the level of ordinary skill. This is an essential finding because (as the Guidelines point out) a finding as to the level of ordinary skill may be used as a partial basis for a resolution of the issue of obviousness. The person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. Factors that may be considered in determining the level of ordinary skill in the art include:

(1) "Type of problems encountered in the art;"

(2) "prior art solutions to those problems;"

(3) "rapidity with which innovations are made;"

(4) "sophistication of the technology;" and

(5) "educational level of active workers in the field."

Guidelines, 72 Federal Register at 57528, citing[2] *In re GPAC*, 57 F.3d 1573, 1579, 35 USPQ2d 1116, 1121 (Fed. Cir. 1995) and *Custom Accessories, Inc.* v. *Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962, 1 USPQ2d 1196, 1201 (Fed. Cir. 1986). In a given case, every factor may not be present, and one or more factors may predominate. Id.

[2] See note 30 of the *Guidelines*.

In the present case, Applicant has presented claims to a device classified in Class 257 (Semiconductor Devices). Considering the five enumerated factors in order, it is noted that:

1) The types of problems encountered in Class 257 typically are highly complex, involving questions of electrodynamics, thermodynamics, crystallography, and quantum mechanics.

2) Prior art solutions to the problems presented in this field demonstrate thinking of the highest order. Many prior art solutions in this field have won Nobel prizes. Over a half century or more, the Nobel Prize Committee has recognized[3] the extraordinary nature (and high value, both commercially and in terms of quality of life) of prior art solutions to complex problems in this field made by individuals such as John Bardeen, William Schockley, Jack Kilby, Leo Esaki, Nick Basow, Zhores Alferov, Pierre-Gilles de Gennes, Herbert Kroemer, and perhaps a few more this writer has overlooked. Note, for example, that the most recent Nobel Prize in physics went to Albert Fert and Peter Grünberg for an innovative solution to the problem of Giant Magnetic Resonance, a solution now incorporated into many semiconductor memory devices.

3) Innovations in Class 257 are made with extremely high rapidity (see, e.g. “Moore’s Law”).

4) Technology used to make and practice inventions in this field are highly sophisticated. Some “fabs” (as those of skill in the art call the factories for making

these devices) now cost in excess of six billion dollars each[4], and perform hundreds of millions of operations per hour.

5) Finally, the educational level of active workers in this field is extremely high – Ph.D.s are common, and a bachelor's degree in engineering is the absolute minimum educational level of workers in this field.

In short, the level of ordinary skill in this field is extremely high. In *KSR* (while considering an invention involving the substitution of one simple mechanical linkage for another), the Supreme Court cautioned, "A person of ordinary skill is also a person of ordinary creativity". *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1742, 82 USPQ2d 1385, 1397 (2007). Had the Court been looking at 1) the scientific complexity of problems encountered in the semiconductor arts, 2) the variety of extraordinarily valuable (from lifestyle-changing, such as high-speed communications and computing, to handy devices such as IPods and cellphones) and difficult solutions to challenging problems that have been accomplished in the semiconductor art in recent years, 3) the extreme rapidity of advances in this art, 4) the highly sophisticated "fabs" used to build semiconductor devices, and 5) the high educational level of persons practicing this art, the Court might have said that in the semiconductor arts (compared to simple mechanical arts such as KSR's) the person of ordinary skill is a person of extraordinary creativity.

---

[3] For example, see "Presentation Speech, 2000 Nobel Prize, http://nobelprize.org/nobel_prizes/physics/laureates/2000/presentation-speech.html

[4] See, e.g., "Trying to Put New Zip Into Moore's Law", New York Times, 2/24/2008 (http://www.nytimes.com/2008/02/24/business/24proto.html?_r=1&oref=slogin)

Next, we consider the first and second factual findings required by *Graham*. With regard to claim 6 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 having a first diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18, and a second diffusion region 24 a Negative Differential Resistance (NDR) device connected between the second diffusion region 24 and a reference potential line 19, the device including an anode and a cathode. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claim 7 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an n-channel access transistor 12 on a bulk semiconductor substrate P-sub, the n-channel access transistor 12 having a first n-type diffusion region (not numbered; seen directly under bit line 18) connected to a bit line 18 and a second n-type diffusion region 24 and a Negative Differential Resistance (NDR) device having an n-type anode connected to a device reference potential line 19 and a p-type cathode in contact with the second n-type diffusion region 24. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 20, 21, 25, 26, and 32, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 including an n-channel transistor on a bulk semiconductor substrate P-sub, including a body region (bulk substrate P-sub) a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to a bit line 18 a

second diffusion region 24 separated from the first diffusion region by a channel area in the body region (bulk substrate P-sub) a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14), the gate 14 electrically connected to a word line a Negative Differential Resistance (NDR) device, including an anode and a cathode, the device being connected between the second diffusion region 24 and a reference potential line 19, wherein the device has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the device and the memory cell is operative to store and sense a charge in the second diffusion region 24 that is representative of a memory state. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 33,34,37, and 39, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 formed in a bulk semiconductor structure, the access transistor 12 including a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and further including a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region is connected to a bit line 18 and the gate 14 is connected to a first word line and a vertically-oriented gate-controlled Negative Differential Resistance (NDR) device connected between a reference potential line 19 and the second diffusion region 24, the device including an anode and a cathode, and an operably positioned gate 20, the gate 20 being connected to a second

word line WL1. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 63-65, 67, 69, and 71, the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising an access transistor 12 including an n-channel transistor, a first diffusion region (not numbered; seen directly under bit line 18) separated from a second diffusion region 24 by a channel region, and a gate 14 separated from the channel region by a gate insulator (not numbered; seen under gate 14), wherein the first diffusion region is connected to a bit line 18 and the gate 14 is connected to a first word line; and a vertically-oriented Negative Differential Resistance (NDR) device connected between a reference potential line 19 and the second diffusion region 24, the NDR device including an n-type anode and a p-type cathode, wherein the device has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the device and wherein the access transistor 12 and the device are on a bulk semiconductor substrate P-sub. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

With regard to claims 72-74 and 77 the scope and content of the prior art includes, in the Nemati et al. disclosure, a description of a memory cell comprising a memory array, including a plurality of memory cells in rows and columns a number of word lines, each word line connected to a row of memory cells a number of bit lines, each bit line 18 connected to a column of memory cells at least one reference line to provide a reference potential to the memory cells control circuitry, including word line

select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations, wherein each memory cell includes an access transistor 12, including a body region (bulk substrate P-sub), a first diffusion region (not numbered; seen directly under bit line 18) electrically connected to one of the bit lines, a second diffusion region 24 separated from the first diffusion region by a channel area in the body region (bulk substrate P-sub), and a gate 14 separated from the channel area by a gate insulator (not numbered; seen under gate 14) and electrically connected to one of the word lines and a vertically-oriented Negative Differential Resistance (NDR) device, including an anode and a cathode, the device being connected between the second diffusion region 24 and a reference line (reference potential line 19), wherein the device has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the device, wherein the memory cell is adapted to store a charge in the second diffusion region 24 of the access transistor 12 to indicate a stable memory state and wherein the device includes a gate-controlled device and the memory device is adapted to gate the gate-controlled device to enhance switching between memory states, wherein the vertical-oriented device is at least partially formed in the floating body of the access transistor 12. Note figures 1-3, 6-8, column 4 lines 1-67, column 5 lines 1-6, and column 6 lines 6-58 of Nemati et al.

The applicant's claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 do not distinguish over the Nemati et al. reference regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the

device per se is relevant, not the recited functions of using the floating node for storing a charge indicative of a memory state of the memory cell.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip opinion[5], page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("'[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and

[5] Available at the BPAI website as http://www.uspto.gov/web/offices/dcom/bpai/prec/fd074423.pdf

Leggett & Platt Inc. v. VUTEk Inc., 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that Nemati et al.'s device is capable of using the floating node for storing a charge indicative of a memory state of the memory cell, because a comparison of Applicant's specification to Nemati et al.'s disclosure reveals that Nemati et al. discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function(s) of using the floating node for storing a charge indicative of a memory state of the memory cell.

Because it is reasonable to predict that assume that Nemati et al.'s device is capable of performing the claimed function, the burden shifts to Appellant to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

The difference between the prior art memory cell disclosed by Nemati et al. and the claimed device is that, where the claim requires a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode, Nemati et al.'s memory cell includes a negative differential resistance NPNP thyristor device.

However, Krivokapic discloses a negative differential resistance diode including an n/i/p diode having an n+ anode 204, a p cathode 206, and an intrinsic region 208 between the anode 204 and cathode 206. Note figure 5, column 3 lines 61-67, and column 4 lines 1-6 of Krivokapic.

The n/i/p diode of applicant's claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 does not distinguish over that of the Krivokapic reference regardless of the claims' reciting the performing of certain function(s) using the claimed diode, because only the device per se is relevant, not the recited functions of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte* Smith, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here,

the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip opinion, page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("'[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that Krivokapic's n/i/p diode is capable of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode, because a comparison of Applicant's specification to Krivokapic's disclosure reveals that Krivokapic discloses a diode that is apparently identical to the diode Applicant describes as being capable of performing the function(s) of using the geometry of intrinsic region of the diode for assisting with stabilizing the memory state of the memory

cell and allowing the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode.

Because it is reasonable to predict that assume that Krivokapic's diode is capable of performing the claimed function, the burden shifts to Appellant to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

The question is, taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art, would it have been obvious to achieve the invention of claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 by substituting the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for Nemati et al.'s negative differential resistance NPNP thyristor device?

To reject a claim on the basis of the rationale expressed in section IIIB of the *Examination Guidelines*, Office personnel first must resolve the Graham factual inquiries (as has just been done). Office personnel must then articulate the following:

> (1) a finding that the prior art contained a device (method, product, etc.) which differed from the claimed device by the substitution of some components (step, element, etc.) with other components;
>
> (2) a finding that the substituted components and their functions were known in the art;
>
> (3) a finding that one of ordinary skill in the art could have substituted one known element for another, and the results of the substitution would have been predictable; and
>
> (4) whatever additional findings based on the *Graham* factual inquiries may be necessary, in view of the facts of the case under consideration, to explain a conclusion of obviousness.

As explained above, Nemati et al. discloses a device (a memory cell) that differed from the claimed device only by the substitution of some components (a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region

between the anode and cathode) for other components (a negative differential resistance NPNP thyristor device). Krivokapic discloses that the substituted components and their functions were known in the art. Further, Krivokapic discloses that those of skill in the art were familiar with a negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode where tunneling occurs through a potential barrier having a very narrow width, so that the frequency response of a resonant tunneling device is not limited by the diffusion or transit time of charge carriers. Instead, the frequency response is limited only by the circuit capacitance and impedance of the device, generating an improved response over the negative differential resistance NPNP thyristor device used in Nemati et al.'s memory cell. From the similarities between the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode and Nemati et al.'s negative differential resistance NPNP thyristor device, one of skill in the art would have been able to conclude that negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode could have substituted for the negative differential resistance NPNP thyristor device of Nemati et al.'s memory cell. One of skill in the art would have had reason to predict (based on its functioning in Krivokapic's disclosure) that negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode would have continued functioning in Nemati et al.'s memory cell much as it did in Krivokapic's disclosure, and that after the substitution, Nemati et al.'s memory cell would continue functioning in the manner disclosed by Nemati et al. It would therefore have been

obvious to a person having skill in the art to modify Nemati et al.'s memory cell by substituting the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for Nemati et al.'s negative differential resistance NPNP thyristor device.

The Guidelines point out that the both the Graham and KSR decisions require Office personnel to evaluate objective evidence relevant to the issue of obviousness. Such evidence, sometimes referred to as "secondary considerations," may include evidence of commercial success, long-felt but unsolved needs, failure of others, and unexpected results. The evidence may be included in the specification as filed, accompany the application on filing, or be provided in a timely manner at some other point during the prosecution. The weight to be given any objective evidence is decided on a case-by-case basis. The mere fact that an applicant has presented evidence does not mean that the evidence is dispositive of the issue of obviousness.

For evidence of unexpected results, one must rely solely on evidence supplied by Appellant. Appellant has actually made the claimed combination. Evidence of differences between results of the actual functioning of the claimed combination and the results of the functioning one of skill in the art would have had reason to predict (i.e., the "expected results") must necessarily come from one who has actually made the combination. A clear case of unexpected results would be if the claimed combination of prior art elements did not in fact perform according to their established functions in a predictable fashion; a result sometimes referred to as "synergy". See *Anderson's-Black Rock v. Pavement Co.* 396 U.S. 57, 61 (1969) (note that the *Anderson's-Black Rock*

opinion does not actually employ the word "synergy"). However, the Guidelines make it clear that any type of unexpected results (and indeed any type of secondary considerations) must be considered.

Appellant's specification, however, does not include any evidence of secondary considerations. Appellant discloses that the claimed combination "may" be made; Appellant does not disclose any unexpected results or indeed any results at all.

(10) Response to Argument

It is argued, at page 14 of the brief, that "Nemati et al indicate that there are different NDR devices and that these different NDR devices have different basis for operation such as a bipolar transistor and quantum-effect devices (col. 3 lines 51 to col. 2 line 26) [or] for power switching (col. 2 lines 13-26, 58-61)." All of this is another way of saying that Nemati discloses multiple embodiments, at least one of which is totally irrelevant to the issue at hand. The issue at hand is whether the claimed memory device is obvious over a single disclosed embodiment of Nemati et al.: the "cell consist[ing] of two elements: a PNPN-type NDR device 10 and an NMOS-type access (or pass) transistor 12" described at column 4 lines 13-25 and shown in figures 1 and 2. The only question (taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art) is, would it have been obvious to achieve the invention of claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 by substituting the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for the "PNPN-type NDR device 10" of Nemati et al.'s figure 2?

Appellant makes much of the fact that Nemati et al. disclose (see title) an “NDR device” and “its applications in high-density high-speed memories” and “in power switches”. However, why Nemati et al. chose to disclose the power thyristor of their figure 8 in the same disclosure as the memory device of their figures 1-2 is irrelevant. It is just as irrelevant as the (perhaps more intriguing) of why Appellants “inventive” figure 3B is virtually identical to Nemati et al.’s figure 2.

Note that at column 7 lines 16-30, Nemati et al. state, "various modifications and changes may be made to the present invention [including] interchanging P and N regions in the device structures and/or using PMOSFETS rather than NMOSFETS.” If one were to perform Nemati et al.’s disclosed step of “interchanging P and N regions in the device structures” in Nemati et al.’s figure 2, Appellant's figure 2B would be produced. If one were to perform Nemati et al.’s disclosed step of “using PMOSFETS rather than NMOSFETS” in Nemati et al.’s figure 2, Appellant's figure 5B would be produced. If one were to perform Nemati et al.’s disclosed steps of “interchanging P and N regions in the device structures” and “using PMOSFETS rather than NMOSFETS” in Nemati et al.’s figure 2, Appellant's figure 4B would be produced.

However, whether "various modifications and changes may be made” to Nemati et al.’s disclosed figures to achieve the multiple figures disclosed by Appellant (although it explains the ease with which one of skill in the art could use Nemati et al.’s disclosure to envision[6] many different embodiments of the same basic disclosure) is irrelevant. The obviousness or non-obviousness of Appellant’s figures in view of Nemati et al.’s

[6] And, in Appellant’s case, claim.

figure 2 is no more at issue here than Appellant's proposal that Appellant's figures should be compared to the power thyristor of Nemati et al.'s figure 8. The issue on appeal is whether (taking into account the high level of education, skill, and creativity of one of ordinary skill in the semiconductor art) it have been obvious to achieve the invention of Appellant's claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 by substituting the negative differential n/i/p diode having an n+ anode, a p cathode, and an intrinsic region between the anode and cathode taught by Krivokapic for the "PNPN-type NDR device 10" of Nemati et al.'s figure 2.

It is argued, at page 15 of the brief, that "The Krivokapic reference was cited for the first time by the Office in the Final Office Action". This is true. Citation to Krivokapic was necessitated by Appellant's 7/9/08 amendment, where claims 1, 6, 7, 20, 33, 63, and 72 were each amended to include the language: "wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without gating the diode". Prior to claims 1, 6, 7, 20, 33, 63, and 72 being amended to exclude gated negative differential n/i/p diodes, Appellant's claims were considered obvious in view of the gated negative differential n/i/p diodes of figures 2 and 3 of Baba 5,686,739. This fact is reflected in the record, in the rejection mailed 4/9/08 and in Appellant's 7/9/08 response.

It is argued, at page 16 of the brief, that "A person of ordinary skill in the art in semiconductor technology is a person of ordinary creativity in the semiconductor technology. As identified in MPEP 2141.03: "A person of ordinary skill in the art is also a person of ordinary creativity, not an automaton." KSR International Co. v. Teleflex Inc.,

550 U.S. __ , 82 USPQ2d 1385, 1397 (2007). The "hypothetical 'person having ordinary skill in the art' to which the claimed subject matter pertains would, of necessity have the capability of understanding the scientific and engineering principles applicable to the pertinent art." Ex parte Hiyamizu, 10 USPQ2d 1393, 1394 (Bd. Pat. App. & Inter. 1988)". All of this is quite true and correct, as far as it goes.

However, prior to *KSR*, the "level of skill" analysis was largely irrelevant in the face of an overweening need to find a "suggestion of the desirability" of the claimed combination. See *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999), as cited in part I ("THE PRIOR ART MUST SUGGEST THE DESIRABILITY OF THE CLAIMED INVENTION") of § 2143.01 of the now-discarded 5th version[7], 8th edition of the MPEP. In affirming a non-obviousness finding using the TSM test criticized as "too rigid" by the KSR Court, the *Al-Site* court wrote, "VSI is unable, however, to point to any specific teaching or suggestion for making this combination. VSI instead relies on what it presumes is the level of knowledge of one of ordinary skill in the art at the time of the invention." Note that *KSR* specifically references *Al-Site*, without enthusiasm for its teachings, at 82 USPQ2d, page 1391.

Recognizing the KSR Court's disapproval of the Federal Circuit's putting its own TSM test ahead of the Graham Court's requirement of at least partial reliance on level of skill in the art, the Guidelines[8] state, "Any obviousness rejection should include, either explicitly or implicitly in view of the prior art applied, an indication of the level of

[7] published August 2006 (nine months before KSR) and superseded September 2007 (four months after KSR). An archived copy of the 5th revision of Edition 8 of Chapter 2100 is available at http://www.uspto.gov/web/offices/pac/mpep/old/E8R5_2100.pdf.

ordinary skill. A finding as to the level of ordinary skill may be used as a partial basis for a resolution of the issue of obviousness." 72 F.R. at 57528. The Guidelines describe the "five-factor" method first laid out in *Custom Accessories, Inc.* v. *Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962, 1 USPQ2d 1196, 1201 (Fed. Cir. 1986), used with enthusiasm through the 1980's, and discarded as irrelevant in the 1990's as the courts (and the MPEP) came to the conclusion that the only possible obvious combination was a combination that was desirable irrespective of the level of skill in the art. The Examiner has used the "five-factor" test, as laid out in the Guidelines, to attempt to approximate the level of skill in this art.

It is argued, at page 17 of the brief, "All NDR devices are not created equally; therefore it is not proper to assert "substitution" as a rationale for combining the references". When Appellant argues that the "simple substitution" rationale is improper, Appellant disagrees with the *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme Court Decision in KSR International Co. v. Teleflex Inc.*, which states, "The rationale to support a conclusion that the claim would have been obvious is that the substitution of one known element for another would have yielded predictable results to one of ordinary skill in the art at the time of the invention." 72 Federal Register 57526, 5730. Appellant also disagrees with MPEP § 2143, which also states (at part "B"), "The rationale to support a conclusion that the claim would have been obvious is that the substitution of one known element for another yields predictable results to one of ordinary skill in the art." When Appellant argues that the

---

[8] *Examination Guidelines for Determining Obviousness Under 35 U.S.C. 103 in View of the Supreme*

"simple substitution" rationale is improper, Appellant disagrees with precedential BPAI law: "Because this is a case where the improvement is no more than 'the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for improvement,' *KSR*, 127 S.Ct. at 1740, 82 USPQ2d at 1396, no further analysis was required by the Examiner."*Ex parte* MARY SMITH, 83 USPQ2d 1509[9], 1518 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) citing *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. —; 127 S.Ct. 1727, 82 USPQ2d 1385 (2007). Finally, when Appellant argues that the "simple substitution" rationale is improper, Appellant disagrees with *KSR*, which states, "when a patent claims a structure already known in the prior art that is altered by the mere substitution of one element for another known in the field, the combination must do more than yield a predictable result". *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. —; 127 S.Ct. 1727, 1734, 82 USPQ2d 1385, 1395 (2007).

If it had been possible for the Examiner to accept Appellant's argument that the "simple substitution" rationale is improper (in the face of contrary opinions from the published *Guidelines*, the MPEP, the precedential BPAI opinion in *Smith*, and *KSR*) the Examiner would have withdrawn the rejection, and this appeal would have been unnecessary.

In support of his argument that it is improper to postulate simply substituting of one NDR device for another NDR device in a memory application, Appellant asserts

---

Court Decision in KSR International Co. v. Teleflex Inc., 72 Federal Register 57526 et seq., cited above.

[9] The Examiner is informed that Board members may no longer have access to USPQ (the only journal in which Smith is published) A slip opinion of Ex parte Smith is available at http://www.uspto.gov/web/offices/dcom/bpai/prec.htm.

that Nemati's memory device is a "high current density thyristor". This assertion is not supported by the evidence of record. Nemati et al. discloses a power (high current density) thyristor at column 6 lines 59-67 and in figure 8. This thyristor is not suited for use in a memory device because every thyristor in the entire chip has a common cathode 38 on the backside of the chip. This cathode would not be readily accessible to the access transistor 12 and bitline 18 on the frontside of the memory chip shown in figure 2. Further, because the cathodes of all the thyristor "cells" in figure 8 are shorted to each other, these thyristors (although each readily contributes to the "high current density" of figure 8's power thyristor) could not be separately accessed to form separate memory cells. "NDR device 10", shown in Nemati et al's figures 1 and 2, is a completely different device from the "high current density thyristor" of Nemati et al's figure 8, as can readily be seen by comparing the figures.

The simple fact is that (as evidenced by the title of the Nemati et al. patent) Nemati et al. disclose two separate and distinct embodiments:

1) A first embodiment, the "array of memory cells" of the embodiment described at column 2 lines 49-57, having NDR devices with current capacities suitable for memory cells.

2) A second embodiment, the "power switch structure" of the embodiment described at column 2 line 58 through column 3 line 3. This device (as shown in figure 8) is configured to achieve a high current density, but is not suited as a memory cell.

Because Nemati et al. disclose two separate embodiments it is possible to examine two completely different questions:

1) Would substituting Krivokapic's NDR n/i/p diode into the "array of memory cells" of the first embodiment (best illustrated in Nemati et al.'s figures 1 and 2) yield predictable results?

2) Would substituting Krivokapic's NDR n/i/p diode into the "power switch structure" of the second embodiment (best illustrated in Nemati et al.'s figure 8) would yield predictable results?

The Examiner has examined question 1 (whether substituting Krivokapic's NDR n/i/p diode into Nemati et al.'s "array of memory cells" would yield predictable results) and concluded that the answer is "yes". Appellant urges the Board to ignore the Examiner's findings relative to question 1, and take up question 2, *de novo*. However, question 2 is irrelevant to the issue of whether claims 1-4, 6, 7, 20, 21, 25, 26, 32-34, 37, 39, 63-65, 67, 69, 71-74, and 77 are obvious. Substituting Krivokapic's NDR n/i/p diode into the "power switch structure" of Nemati et al.'s figure 8 (regardless of whether this would have been yielded predictable results) would not produce the claimed invention. Nemati et al.'s "power switch structure" (a completely separate device from Nemati et al's "NDR device 10", as can readily be seen) is not suited to memory cell construction.

At page 17 Appellant asserts, "[Because an] RTD allows 100% transmission at predetermined energy levels…. one of ordinary skill would not believe that an RTD could be simply substituted for the thyristor in the memory cell of Nemati et al." This

assertion mischaracterizes the Krivokapic disclosure. Krivokapic simply states, “RTDs are two terminal devices with conduction carriers through potential barriers to yield current-voltage curves with portions exhibiting negative differential resistance.” Note column 1 lines 33-35 of Krivokapic. Nowhere does Krivokapic (or any reference of record) state that RTDs allow 100% transmission at predetermined energy levels. Appellant appears to have made this “fact” up out of whole cloth. However, even if it were true, at best Appellant's “fact" would have something to do about the mechanism by which RTDs such as those of Krivokapic’s figure 3 and 5 achieve “current-voltage curves with portions exhibiting negative differential resistance.” Applicant’s “fact” would not change the ultimate fact, adduced from evidence in the record (column 1 lines 33-35 of Krivokapic): RTDs exhibit the same sort of negative differential resistance Nemati et al.'s “PNPN-type NDR device” does. Note that although Nemati et al. state that their memory cell “can [emphasis added] be referred to as thyristor based SRAM cell” (column 4 lines 11-12), Nemati et al. do not themselves refer to their NDR memory device as a “thyristor”. Nemati et al. refer to the NDR device of their memory cell as “PNPN-type NDR device 10”, once (column 4 line 13), and thereafter refer to it as “NDR device 10”.

It is asserted, at page 18 of the brief, that “There is a different structure (e.g. geometry of the intrinsic region) between the diode of the present application and the RTD of Krivokapic”. This statement is not supported by the evidence of record. The geometry of the intrinsic region of the vertical RTD of Krivokapic’s figure 3 is identical to the geometry of the intrinsic region of the vertical charge-enhanced n/i/p diode of

Appellant's figure 13. The geometry of the intrinsic region of the lateral RTD of Krivokapic's figure 5 is identical to the geometry of the intrinsic region of the lateral charge-enhanced n/i/p diode of Appellant's figure 1A.

It is argued, at page 18 of the brief, that "The intrinsic region in the diode in the present claims allows the claimed memory cell to hold charge." This is an argument made many times (in many forms) since *In re Swinehart* (439 F.2d 210, 169 USPQ 226 (CCPA 1971) first made it clear that it was possible to define a device "by what it *does* rather than what it *is*." For instance, In *In re Ludtke*, 441 F.2d 660, 663-64, 169 USPQ 563, 565-67 (CCPA 1971), claim 1 was directed to a parachute canopy having concentric circumferential panels radially separated from each other by radially extending tie lines. The panels were separated "such that the critical velocity of each successively larger panel will be less than the critical velocity of the previous panel, whereby said parachute will sequentially open and thus gradually decelerate". A prior art (Menget's) set of tie lines were judged inherently capable of achieving the function of providing said critical velocities, based on their similarities to Ludtke's disclosed tie lines. The court upheld the rejection as establishing a *prima facie* case of anticipation, finding, further, that applicant had not met his burden (established by the *prima facie* case) of showing that Menget did not possess the functional characteristics of the claims.

See also *In re Schreiber*, 128 F.3d 1473, 44 USPQ2d 1429 (Fed. Cir. 1997) ("[N]othing in Schreiber's [applicant's] claim suggests that Schreiber's container is of a 'different shape' than Harz's [patent]. In fact, [ ] an embodiment according to Harz (Fig.

5) and the embodiment depicted in Fig. 1 of Schreiber's application have the same general shape. For that reason, the examiner was justified in concluding that the opening of a conically shaped top as disclosed by Harz is inherently of a size sufficient to 'allow [ ] several kernels of popped popcorn to pass through at the same time' and that the taper of Harz's conically shaped top is inherently of such a shape 'as to by itself jam up the popped popcorn before the end of the cone and permit the dispensing of only a few kernels at a shake of a package when the top is mounted to the container.' The examiner therefore correctly found that Harz established a prima facie case of anticipation"), as cited in MPEP 2112, part IV.

The present case presents similar facts to those presented in *Ludtke* and *Schreiber*. In his specification, Appellant describes an intrinsic region that (like Ludtke's tie lines and Schreiber's container) is not described as having any particular critical length, breadth, depth, or shape, yet is nonetheless capable of "holding charge". Under these circumstances, it is reasonable to predict that Krivokapic's intrinsic region (which is exactly like Appellant's intrinsic region, physically, in that it, too, has no particular length, breadth, depth, or shape) is also capable of "holding charge". When a device is claimed using "functional language" and it is reasonable to predict that the prior art is inherently capable of performing the recited function, the burden shifts to the applicant to provide suitable evidence that this is not in fact the case. See MPEP § 2112, part V.

It is argued, at page 18 of the brief, that "The Office makes an improper inference when asserting that Krivokapic discloses that the substituted components and their functions were known in the art (page 19 lines 9-17)."

It is difficult to understand what Appellant means by this. As a matter of law, the "art" is presumed to know every relevant teaching in the field. *In re Winslow,* 365 F.2d 1017, 1020, 151 USPQ 48, 51 (CCPA 1966). ("Section 103 requires us to presume full knowledge by the inventor[10] of the *prior* art in the field of his endeavor"). Since Krivokapic teaches a device relevant to the subject of the claims (a memory device) including a negative differential resistance n/i/p diode having an n+ anode 204, a p cathode 206, and an intrinsic region 208 between the anode 204 and cathode 206, the person having skill in the art is presumed, as a matter of law, to have known of this diode. Since Krivokapic teaches that this n/i/p diode functions as a two terminal device yielding a current-voltage curve with portions exhibiting negative differential resistance, the person having skill in the art is presumed, as a matter of law, to have known of this function.

By "The Office makes an improper inference when asserting that Krivokapic discloses that the substituted components and their functions were known in the art", does Appellant intend to argue that the law requires the substituted components and their functions to have been disclosed more than once (here, they are only disclosed once) before it can be said that they were "known in the art"? If Appellant is of the opinion that "substituted components and their functions" must be disclosed more than

[10] In a later opinion, Judge Rich (the author of the *Winslow* opinion) corrected himself on this reference to the person of skill in the art as "inventor". See *Kimberly-Clark Corp. v. Johnson & Johnson*, 745 F.2d 1437, 1446, 223 USPQ 603, 613 (Fed.Cir. 1984), (explaining, it is not "the inventor or applicant or patentee, but that it is *the hypothetical person of ordinary skill in the art* who is referred to in §103 of the 1952 Patent Act who must be presumed to have, or is charged with having, knowledge of all material prior art")

once to be "known in the art", how many disclosures will satisfy the legal requirement, in Appellant's opinion? Two? Three? Nine? Ninety? Appellant does not say.

Appellant continues, "An RTD is known. However, substituting an RTD for a thyristor, particularly in a memory circuit illustrated in Nemati et al., is not known." Appellant's argument begs the ultimate question of obviousness – Appellant in essence argues that a thing is not obvious until a reference teaches that it exists. If there was a reference that made known a memory cell substituting an NDR n/i/p diode (such as Krivokapic's n/i/p diode) for Nemati et al.'s PNPN-type NDR device, that reference would be a 102 reference, and the obviousness analysis would be moot.

It should be noted, again, that Nemati et al. never actually refer to their NDR memory device as a "thyristor" (although they state, column 4 line 12, that others can refer to the disclosed memory cell as "thyristor based", should they choose to). Nemati et al. refer to the NDR device of their memory cell as "PNPN-type NDR device 10", once (column 4 line 13), and thereafter refer to it as "NDR device 10". To match the reality of the Nemati et al. disclosure, Appellant would have asserted, "Substituting an RTD for a ~~thyristor~~ PNPN-type NDR device, particularly in a memory circuit illustrated in Nemati et al., is not known". For full disclosure, Appellant might have written, "Even though Nemati et al. disclose that the PNPN-type NDR device in their memory cell is chosen for its NDR properties, and even though Krivokapic discloses that his RTD has NDR properties, substituting an RTD for the PNPN-type NDR device in the memory circuit illustrated in Nemati et al. is not known."

In *In re Wheatley*, No. 2006-1400 (a Federal Circuit affirmance of a Board decision, made without opinion (Rule 36) about three months before KSR was decided), one reference taught polarizing birefringeant layers of PET (a polarizing plastic) alternating with layers of silicon oxide. Another reference disclosed that PEN (another plastic) was equally polarizing to PET. The second reference did not compare the polarizing properties of PEN to those of PET in layers alternating with silicon oxide; the second reference only compared the properties of the two plastics in bulk samples. The issue on appeal was whether is would have been obvious to achieve the claimed invention by simply substituting PEN for the PET of the first reference.

At Federal Circuit oral arguments, counsel for Wheatley argued, "The problem facing the inventors is to find the right combination of materials for these adjacent layers that can be co-extruded and rendered bi-refringeant with that refraction index mismatch to get the reflected polarization back... I don't agree that improving polarization in the abstract was the problem." On hearing this, one member of the court commented: "It seems to me what you are suggesting is, the only time you could have an effective prima facie 103 rejection is if the Patent Office came up with effectively a 102 reference that showed not only the improved film but the improved film within the multilayered co-extruded framework. But I don't think our precedent requires that, in any way, shape, or form." *In re Wheatley*, No. 2006-1400, oral arguments, 2/18/2007, http://oralarguments.cafc.uscourts.gov/mp3/2006-1400.mp3 (the court's comment can be heard at about the nine minute, fifty second point in the audio transcript).

Appellant appears to argue that the only time one could have an effective prima facie 103 rejection in the present case is by coming up with effectively a 102 reference that shows not only Krivokapic's NDR n/i/p diode but the NDR n/i/p diode within Nemati et al.'s memory cell framework. The Examiner, on the other hand, finds wisdom in the (admittedly offhand) remark of the *Wheatley* court. It is unlikely that Federal Circuit precedent requires that a reference teach a device formed by actually making a substitution, before the substitution can be found obvious.

Appellant argues further, at page 18 of the brief, that "The Office has not shown why one would gate a resonant tunneling diode with a diode gate. Various claims (e.g. claim 6) recite that the diode includes a diode gate."

Since Appellant does not claim a resonant tunneling device, the Office is under no obligation to show one, gated or otherwise. As to showing the obviousness of a combination of a gated NDR n/i/p diode with the other elements of claim 6 (all of which are taught by Nemati et al.), the Office did so on pages 57-59 of the rejection mailed 4/9/08. There, it was established that the similarities between the I/V response curve of a gated NDR n/i/p diode taught by Baba 5,686,739 and the I/V response curve of Nemati et al.'s gated PNPN NDR device would have led one of skill in the art to conclude that Baba's gated NDR n/i/p diode could have been substituted for Nemati et al.'s gated PNPN NDR device with predictable results.

On 7/9/08 Appellant amended claim 6 to require that its n/i/p diode <u>not</u> be gated, using the language, "wherein the diode has a structure to allow the memory cell to switch memory states using a forward or reverse bias voltage across the diode without

gating the diode". The combination of Nemati et al. and Krivokapic teaches a memory device with an un-gated n/i/p diode. However, this is precisely what Appellant's amended claim language demands. Note that in his 7/9/08 remarks (page 22) Appellant stated, "In contrast [to Baba], Applicant claims a diode [where] a diode gate is not necessary to switch states."

Between pages 19 and 24 of the brief Appellant repeats the following combination of conclusory statements seven times (once for each independent claim): "The cited portions of Nemati et al. and Krivokapic, in conjunction with the rationale for the rejection contained in the Final Office action, do not provide the rational underpinning required to support the legal conclusion of obviousness. The Office has not established a rationale, sufficient to support the assertion that it would be obvious to substitute a RTD of Krivokapic for the thyristor in Nemati et al. for use in conjunction with the access transistor and reference voltage (V-F) in Nemati et al. Further, the Office has not shown that the RTD would be able to hold a charge on the floating node in the memory cell of Nemati et al." In each of these seven repetitions, Appellant persists in supplying no basis, in law or in fact, for this statement. Appellant appears to have simply repeated the same conclusory statement seven times over.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Conclusion

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Thomas L Dickey/

Primary Examiner, Art Unit 2826

Conferees:

/Davienne Monbleau/

Supervisory Patent Examiner, Art Unit 2893

/Darren Schuberg/

TQAS TC 2800